Chip Errata for the IT81202/IT81302 BX/CX version

1. ERR002:

When FIFO2 is enabled on I2C channel C and there is also bus transfer on I2C channel B. Sometimes, channel C may write wrong data to the targeted device.

2. Failure Analysis:

This issue arises because FIFO2 is shared between channel B and channel C.

FIFO2 will be disabled when data access is completed to ensure FIFO is cleared, under this condition FIFO2 is set on channel B by default. Even FIFO2 is set on channel C, the byte counter of FIFO2 may be affected by channel B when enable FIFO2.

3. Impact:

FIFO2 mode can’t be enabled on channel C when channel B is concurrently in used.

4. Proposed Solution:

Disabled FIFO2 on channel C.