Chip Errata for the IT81202 BX Version

ERR001 :

Two consecutive instructions after mul instruction will have chances to miss the data written back to the CPU GPR (General Purpose Register).

Description:

When the mul instruction is in the write back stage, and there is an io read data that also needs to be written back to the GPR at the same time: this will cause problem to write back data of the two consecutive instructions after mul.
This is because the pipeline order of mul will change from “execute -> memory -> write back“ to “execute -> stall -> memory -> write back“.
However, the pipeline order of the two consecutive instructions after mul are not changed as expected.

Impact:

This error can cause GPR store the wrong data.

Workarounds:

The solution to this problem is to put two instructions that do not require write back data after the mul instruction.

Proposed Solution:

Fix in the CX version.